REMARKS/ARGUMENTS

The Applicants originally submitted Claims 1-22 in the application. In the present response, the Applicants have amended Claims 1, 8 and 15. No claims have been cancelled or added. Accordingly, Claims 1-22 are currently pending in the application.

I. Rejection of Claims 1-4 and 8-11 under 35 U.S.C. §102

The Examiner rejected Claims 1-4 and 8-11 under 35 U.S.C. §102(b) as being unpatentable over U.S. Patent No. 5,528,513 to Vaitzblit, *et al.* ("Vaitzblit"). The Examiner asserts that Vaitzblit teaches each and every element of independent Claims 1 and 8. (Examiner's Action, page 2). The Applicants respectfully disagree.

Vaitzblit does not teach managing multitasking in a processor including acknowledging events based on relevance to a currently-active context. (Claims 1 and 8). Instead, Vaitzblit teaches a scheduler for a continuous media file server where scheduling is performed in a hierarchical manner for isochronous, real-time and general purpose tasks. (Abstract). The scheduler determines whether a currently running task needs to be preempted whenever an isochronous task arrives at a server. If the currently running task is a general purpose task or a real-time task, then the arriving isochronous task will preempt the currently running task. If the currently running task is another isochronous task, then the arriving isochronous task will preempt the currently running task if the arriving isochronous task has a higher priority. (Column 4, lines 48-60).

Preempting currently running tasks based on the class and priority of the arriving task, however, does not teach acknowledging events based on relevance to a currently-active context. (Claims 1 and 8). On the contrary, Vaitzblit teaches that regardless of the relevance of the arriving

task to the currently running task, the currently running task will be preempted if the arriving task is an isochronous task and/or an isochronous task with a higher priority than the currently running task. Vaitzblit, therefore, does not disclose each and every element of the claimed invention associated with independent Claims 1 and 8 and Claims dependent thereon. Accordingly, the Applicants respectfully requests the Examiner to withdraw the §102(b) rejection with respect to Claims 1-4 and 8-11.

II. Rejection of Claims 5 and 12 under 35 U.S.C. §103

The Examiner rejected Claims 5 and 12 under 35 U.S.C. §103(a) as being unpatentable over Vaitzblit in view of U.S. Patent No. 6,009,454 to Dummermuth, *et al.* (Dummermuth). The Examiner has cited Dummermuth for teaching instruction counts. (Examiner's Action, page 3). Dummermuth is directed to a multi-tasking operating system for real-time control of industrial processes. (Abstract). Multi-tasking is provided by recognizing that both ladder-type and state-type programs can be considered as simply a collection of individual instructions linked together by an implicit pointer list. (Column 2, lines 48-53).

As discussed above, however, Vaitzblit does not teach each and every element of independent Claims 1 and 8. Furthermore, Vaitzblit does not suggest each and every element of Claims 1 and 8. Dummermuth also does not teach or suggest managing multitasking in a processor including acknowledging events based on relevance to a currently-active context. (Claims 1 and 8). Instead, Dummermuth teaches executing programs according to a fixed number of allocated instructions. (Abstract). Dummermuth, therefore, fails to cure the deficiencies of Vaitzblit.

Since neither Vaitzblit of Dummermuth, individually or in combination, teach or suggest each and every element of independent Claims 1 and 8, the combination of Vaitzblit and Dummermuth fails to establish a *prima facie* case of obviousness regarding dependent Claims 5 and 12 which includes the elements of Claims 1 and 8, respectively. Accordingly, the Applicants respectfully traverse the Examiner's rejection of Claims 5 and 12 under 35 U.S.C. §103(a) and request the Examiner withdraw the rejection with respect to these claims.

III. Rejection of Claims 6 and 13 under 35 U.S.C. §103

The Examiner rejected Claims 6 and 13 under 35 U.S.C. §103(a) as being unpatentable over Vaitzblit in view of U.S. Patent No. 5,239,652 to Seibert, *et al.* ("Seibert"). As discussed above, Vaitzblit does not teach or suggest each and every element of independent Claims 1 and 8. Furthermore, Seibert does not cure the deficiencies of Vaitzblit. Instead, Seibert is directed to reducing the power consumption of a computer by determining when the central processing unit is not actively processing and generating a power-off signal to a control logic circuit. (Abstract). Since the Examiner did not establish a *prima facie* case of obviousness of independent Claims 1 and 8, and Seibert does not cure the deficiencies of Vaitzblit, then the Examiner cannot establish a case of obviousness of dependent Claims 6 and 13. Accordingly, the Applicants respectfully traverse the Examiner's rejection of Claims 6 and 13 under 35 U.S.C. §103(a) and request the Examiner withdraw the rejection with respect to these claims.

IV. Rejection of Claims 7 and 14 under 35 U.S.C. §103

The Examiner rejected Claims 7 and 14 under 35 U.S.C. §103(a) as being unpatentable over Vaitzblit in view of U.S. Patent No. 6,256,659 to McLain, Jr. *et al.* As discussed above, Vaitzblit does not teach or suggest each and every element of independent Claims 1 and 8. Furthermore, McClain does not cure the deficiencies of Vaitzblit. Instead, McClain is directed to performing hybrid preemptive and cooperative multi-tasking by executing a number of logical units of work before interrupting a task. (Abstract). Since the Examiner did not establish a *prima facie* case of obviousness of independent Claims 1 and 8, and McClain does not cure the deficiencies of Vaitzblit, then the Examiner cannot establish a case of obviousness of dependent Claims 7 and 14. Accordingly, the Applicants respectfully traverse the Examiner's rejection of Claims 7 and 14 under 35 U.S.C. §103(a) and request the Examiner withdraw the rejection with respect to these claims.

V. Rejection of Claims 15-18 and 22 under 35 U.S.C. §103

The Examiner rejected Claims 15-18 and 22 under 35 U.S.C. §103(a) as being unpatentable over Vaitzblit in view of U.S. Patent No. 5,713,038 to Motomura. As discussed above, Vaitzblit does not teach or suggest managing multitasking in a processor including acknowledging events based on relevance to a currently-active context as claimed in independent Claim 15. Furthermore, Motomura does not cure the deficiencies of Vaitzblit. Instead, Motomura is directed to a microprocessor that has a register file which allows a higher speed, more flexible, context switching as compared to conventional microprocessors. (Column 3, lines 15-17).

Since Vaitzblit does not teach each and every element of independent Claim 15 and Motomura does not cure its deficiencies, then the Examiner can not establish a *prima facie* case of

obviousness of independent Claim 15 and Claims dependent thereon. Accordingly, the Applicants respectfully traverse the Examiner's rejection of Claims 15-18 and 22 under 35 U.S.C. §103(a) and request the Examiner withdraw the rejection with respect to these claims. Furthermore, a person having ordinary skill in the art would not have been motivated to combining the teachings of Vaitzblit and Motomura since Vaitzblit is directed to controlling tasks in a continuous media file server and Motomura is directed to providing register files to a microprocessor to allow high speed and flexible context switching.

VI. Rejection of Claims 19-21 under 35 U.S.C. §103

The Examiner rejected Claims 19-21 under 35 U.S.C. §103(a) as being unpatentable over Vaitzblit and in further view of Dummermuth, Motomura, Seibert, McClain or a combination thereof. As discussed above, Vaitzblit does not teach or suggest managing multitasking in a processor including acknowledging events based on relevance to a currently-active context as claimed in independent Claim 15. Furthermore, Dummermuth, Motomura, Seibert, McClain or a combination thereof does not cure the deficiencies of Vaitzblit.

Since Vaitzblit does not teach each and every element of independent Claim 15 and Dummermuth, Motomura, Seibert, McClain or a combination thereof does not cure its deficiencies, then the Examiner can not establish a *prima facie* case of obviousness of independent Claims 19-21 which includes each and every element of Claim 15. Accordingly, the Applicants respectfully traverse the Examiner's rejection of Claims 19-21 under 35 U.S.C. §103(a) and request the Examiner withdraw the rejection with respect to these claims.

VII. Conclusion

In view of the foregoing remarks, the Applicants now see all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1-22. Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

HITT GAINES & BOISBRUN, P.C.

J. Joel Justiss
Registration No. 48,981

Dated: 11/11/02

P.O. Box 832570
Richardson, Texas 75083
(972) 480-8800

IN THE CLAIMS:

(1) Kindly amend Claim 1 as follows:

1. (Amended) A context controller for managing multitasking in a processor, comprising:

an event recorder that records occurrences of predetermined events; and

an event acknowledger, associated with said event recorder, that acknowledges ones of said events based on relevance to [an identity of] a currently-active context.

(2) Kindly amend Claim 8 as follows:

8. (Amended) A method of managing multitasking in a processor, comprising the steps of:

recording occurrences of predetermined events; and

acknowledging ones of said events based on relevance to [an identity of] a currently-active context.

(3) Kindly amend Claim 15 as follows:

15. (Amended) A processor, comprising:

an instruction decoder that decodes instructions received into said processor and corresponding to a plurality of tasks;

a plurality of register sets, corresponding to said plurality of tasks, that contain operands to be manipulated;

an execution core, coupled to said instruction decoder and said plurality of register sets, that executes instructions corresponding to an active one of said plurality of tasks to manipulate ones of said operands; and

a context controller for managing multitasking in said processor, including:

an event recorder that records occurrences of predetermined events; and

an event acknowledger, associated with said event recorder, that acknowledges ones of said events based on relevance to [an identity of] a currently-active context.